TITLE

FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN

CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for *FLAT PANEL DISPLAY AND DIGITAL DATA PROCESSING DEVICE USED THEREIN* earlier filed in the Korean Industrial Property Office on the 16th of December 1997 and there duly assigned Serial No. 37478/1997.

BACKGROUND OF THE INVENTION

Field of The Invention

The present invention concerns a flat panel display for receiving display information by means of a digital communication, and a digital processing device for utilizing it to connect to an analog display.

Description of the Related Art

It has been usual for a digital processing device such as a personal computer system to use a CRT (Cathode Ray Tube) for a display. Nowadays, a flat panel display such as an LCD (Liquid Crystal Display) or plasma display is also widely used. Such a flat panel display reproduces the image by converting the video signal received from a host such as a personal computer system to

corresponding digital data.

An LCD system generally includes an ADC (Analog-to-Digital Converter), a PLL circuit (Phase Locked Loop), a video data converter, an LCD driver, and an LCD panel the ADC converts an analog R(red), G(green) and B(blue) video signal to corresponding digital video data. The PLL circuit generates an internal clock signal in response to a synchronizing signal received from a host. The video data converter converts the digital video data according to a clock signal. This is to accommodate the dot and line numbers of the video data supplied to the LCD driver when the resolution provided by the host differs from that of the display. The LCD panel is driven by the LCD driver, displaying the video signal. Such a flat panel display system suffers from the following drawbacks:

The ADC for converting the analog video signal of the host to the digital video signal must perform the sampling operation at the rate of at least twice the frequency of the analog video signal. Additionally, the PLL circuit must have a wide locking range. This causes considerable increase of the overall production cost of the flat panel display. Moreover, a signal loss may frequently occur as well as jittering during analog-to-digital conversion, making the conversion unstable. Further, the allowable frequency range of the input signal is very limited owing to the operational characteristics of the ADC and PLL circuit. In addition, the screen size of the flat panel display is generally so small that it is inconvenient to make a presentation to many people.

The following each disclose features in common with the present invention: U.S. Patent No. 5,608,418 to McNally, entitled *Flat Panel Display Interface For A High Resolution Computer Graphics System*, U.S. Patent No. 5,491,496 to Tomiyasu, entitled *Display Control Device For Use*

With Flat-Panel Display And Color CRT Display, U.S. Patent No. 5,606,348 to Chiu, entitled *Programmable Display Interface Device And Method*, U.S. Patent No. 5,479,183 to Fujimoto, entitled *Apparatus And Method For Detecting An Optical CRT Display Connected To A Computer System*, U.S. Patent No. 5,828,349 to MacHesney *et al.*, entitled *Method And System For Multiplexing And Demultiplexing Video Signals For Graphic Display Monitors In Computer Systems*, U.S. Patent No. 5,841,418 to Bril *et al.*, entitled *Dual Displays Having Independent Resolutions And Refresh Rates*, U.S. Patent No. 5,764,201 to Ranganathan, entitled *Multiplexed Yuv-Movie Pixel Path For Driving Dual Displays*, U.S. Patent No. 5,710,570 to Wada *et al.*, entitled *Information Processing Unit Having Display Functions*, U.S. Patent No. 5,673,058 to Uragami *et al.*, entitled *One-Chip Semiconductor Integrated Circuit Device Capable Of Outputting Analog Color Signal Or Digital Color Signal*, U.S. Patent No. 5,629,715 to Zenda, entitled *Display Control System*, U.S. Patent No. 5.694.141 to Chee, entitled *Computer System With Double Simultaneous Displays Showing Differing Display Images*, U.S. Patent No. 5,579,025 to Itoh, entitled *Display Control Device For Controlling First And Second Displays Of Different Types*, and U.S. Patent No. 5,534,883 to Koh, entitled *Video Signal Interface.*

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a flat panel display which displays digital display information supplied by a digital data processing device.

It is another object of the present invention to provide a flat panel display with means for connecting to an analog display, which may make a convenient presentation to many people.

According to an embodiment of the present invention, a flat panel display for receiving display information including video data and synchronizing data from a host processing digital data in a serial digital communication, comprises: a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a digital-to-analog converter (DAC) for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display.

Preferably, a video data converter is further included to convert the line and dot numbers of the video data so as to correspond to a prescribed display mode when the synchronizing data has a different characteristic from the prescribed display mode. The synchronizing signal generator is accommodated to generate the synchronizing signal corresponding to the display mode.

According to another embodiment of the present invention, there is provided a digital data processing device, which may be used in a flat panel display for displaying display information received from a host processing digital data, and comprises: a transmitter connected to the host to transfer digital display information in serial data, a receiver for reconstructing the display information, a synchronizing signal generator for generating a synchronizing signal by extracting the synchronizing data from the reconstructed display information, a DAC for converting the video data to a corresponding video signal, and an output terminal for externally transferring the synchronizing signal and analog video signal to an analog display. The flat panel display includes the receiver, synchronizing signal generator and output terminal.

Preferably, a video data converter is further included to convert the line and dot numbers of

the video data so as to correspond to a prescribed display mode when the synchronizing data has a different characteristic from the prescribed display mode. The synchronizing signal generator is accommodated to generate the synchronizing signal corresponding to the display mode.

Thus, the host provides the display information as serial digital data, which is transferred to the flat panel display to display the digital video signal, and/or converted to an analog video signal, which is supplied to an analog display to display the analog video signal according to the synchronizing signal.

The present invention will now be described more specifically with reference to the drawings attached only by way of example.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

Fig. 1 is a block diagram for schematically showing the circuit of an earlier LCD system; and

Fig. 2 is a block diagram for schematically showing the circuit of an LCD system provided with means for connecting to a CRT according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram of the LCD system discussed in the Description of the Related Art

above.

The illustrated LCD system includes an ADC 210, a PLL circuit 220, a video data converter 230, an LCD driver 240, and an LCD panel 250. The ADC 210 converts an analog video signal 102 to corresponding to digital video data 212. The PLL circuit 220 generates an internal clock signal in response to a synchronizing signal 104 received from a host 100. The video data converter 230 converts the digital video data 212 according to a clock signal 222. This is to accommodate the dot and line numbers of the video data supplied to the LCD driver 240 when the resolution provided by the host 100 differs from that of the display. The LCD panel 250 is driven by the LCD driver 240 displaying the video signal.

Referring to Fig. 2, a host 300 is provided with a transmitter 310 to transfer display information 312 by means of a digital communication, for example, according to the IEEE 1394 format. The inventive LCD system 400 includes a receiver 410, a video data converter 420, a synchronizing signal generator 430, an LCD driver 240, a RAMDAC 440, an output terminal 450, and an LCD panel 250.

The receiver 410 reconstructs the display information 312 received from the transmitter 310 to provide the video data converter 420 with data 412 including R, G, B video data and a dot clock signal. The video data converter 420, if a conversion of the video data is required, changes the dot and line numbers of the video data to correspond to the resolution supported by the LCD 400, delivering the converted video data 422 to the LCD driver 240. On the other hand, the converted video data 414 is supplied to the RAMDAC 440 to convert to the analog R, G, B video signal 442 delivered to the output terminal 450. Synchronizing data 414 for horizontal and vertical

synchronization is supplied to the synchronizing signal generator 430 to generate a synchronizing signal 432 delivered to the output terminal for the analog display.

The analog display connected to the output terminal 450 may be, for example, a CRT display 500, which comprises an amplifier 510, a deflection signal generator 520, a high voltage generator 530, and a CRT 540. The CRT display 500 receives the analog video signal 442 and synchronizing signal 432 through the output terminal 450. The analog video signal 442 is amplified through the amplifier 510, which supplies the amplified video signal 512 to the CRT 540. The synchronizing signal 432 is transferred to the deflection signal generator 520 to supply the corresponding deflection signal 522 to the CRT 540.

INS D3 Thus, the host 300 supplies serially the digital display data to the LCD 400 to display the image on the LCD panel 250 while the CRT display 500 connected to the output terminal 450 of the LCD 400 receives the analog video signal and synchronizing signal to display the image through the CRT 540.

As described above, the inventive flat panel display does not require a separate ADC because it receives the display information in digital data, and provides means for connecting an analog display.

It should be understood that the present invention is not limited to the particular embodiment disclosed herein as the best mode contemplated for carrying out the present invention, but rather that the present invention is not limited to the specific embodiments described in this specification except as defined in the appended claims.